REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed August 29, 2002.

I. Present Status of Patent Application

Upon entry of this response claims 1-4, 6-7, and 9-10 are pending in the present application. Claims 5 and 8 have been canceled without prejudice, waiver, or disclaimer. Applicants reserve the right to pursue the subject matter of any canceled claims in continuation applications. Claims 1, 3, and 6 have been amended as set forth above, and claims 9 and 10 are newly added. Support for these amendments are found in the specification and in the original claims. No new matter has been added.

II. Objection to the Specification

The Office Action objected to the specification, due to an informality, because "the connections of the third terminals of the first, second and third transistors for receiving the control signal in claim 6 is not disclosed in the specification."

Applicants respectfully disagree. The specification clearly discloses that the connection of the "third terminal of the first transistor device is configured to receive a control signal" (page 3, lines 1-3). Similarly, the specification discloses that the "third terminal of the second transistor is configured to receive a control signal" (page 3, lines 5-6). Finally, the specification discloses that the "third terminal of the third transistor is configured to receive a control signal" (page 3, lines 9-10).

Therefore, Applicants respectfully assert that the specification does not contain the informality suggested in the Office Action. Accordingly, Applicants request that the Examiner reconsider and withdraw the objection to the specification.

III. Claims 6, 7, and 8 Comply With 35 U.S.C. §112, First Paragraph

Claims 6-8 have been rejected under 35 U.S.C. § 112, first paragraph, for the objections cited in the Office Action against the specification. Specifically, the Office Action argues that "the third terminals of the first, second and third transistors are configured to receive the control signal, in claim 6, is not disclosed in the specification." In that these objections are believed to have been overcome, Applicants respectfully request that the rejection of claims 6 and 7 under 35 U.S.C. § 112, first paragraph, be withdrawn.

IV. Claims 3 and 4 Comply with 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 3-5 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Specifically, the Office Action states:

> Regarding claim 3, the recitation "the transistor circuit" on line 10 is indefinite because it is misdescriptive because the "a circuit" is connected to the transistor device instead of to the "transistor circuit".

Applicants respectfully disagree with the assertion in the Office Action that the recitation of the language "the transistor circuit" in claim 3 is indefinite. The term **"transistor circuit"** in claim 3 refers to the entire circuit, for example, as described in Fig. 11 and in the specification as transistor circuit 1100. The term **"transistor device"** refers to an individual transistor, for example, the transistor device 1106 as shown in Fig. 11. The **"a circuit"** and **"the circuit"** refers to a circuit such as inverter circuit 1102 as shown in Fig. 11. Thus, as shown in Fig.11, the inverter circuit is connected to the transistor device as claimed, rather than to the "transistor circuit" as suggested by the Examiner.

However, in the interest of furthering prosecution, Applicants have amended claim 3 to clarify that the "a circuit" and "the circuit" in claim 3 refers to "an inverter circuit" and "the inverter circuit" as described in the specification. The specification provides sufficient detail such that whatever lexicography is used, the "a circuit" and "the circuit" (now "an inverter circuit") is intended to have the property of pulling the connection to ground when a voltage bias is applied to the switch terminals. Further, when no voltage bias is applied to the switch nodes, the circuit pulls the connection to the voltage applied to voltage source terminal.

Applicants wish to clarify that the foregoing amendment has been made for purposes of better defining the invention in response to the rejections made under 35 U.S.C. § 112, and not in response to the rejections made based on a prior art reference. Indeed, Applicants submit that no substantive limitations have been added to the claims. Applicants further submit that this merely cosmetic amendment is non-narrowing and, pursuant to *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831 (2002), no prosecution history estoppel arises from these amendments.

Therefore, Applicants respectfully assert that the language "the transistor circuit" on line 10 of independent claim 3 is not indefinite. Rather, this language clearly points out and distinctly claims the subject matter which Applicants regard as the invention. Accordingly, Applicants request that the Examiner reconsider and withdraw the rejection of independent claim 1 (and claim 2 which depends on claim 1) under 35 U.S.C. §112, second paragraph.

V. Claims 1 and 2 are Patentable Over U.S. Patent No. 4,678,947 to *Huijsing*

The Office Action rejects claims 1 and 2 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,678,947 to *Huijsing* ("the '947 patent"). Specifically, the Office Action argues that figure 2 of the '947 patent shows all of the features of the transistor circuit of

claims 1 and 2. The Office Action further alleges that the last three lines of claim 1 are merely "result" language and "thus may not be used to distinguish over the disclosure" of the '947 patent.

Applicants' claim 1, as amended, recites:

> 1. (thrice amended) A transistor circuit for implementing a switch, comprising:
>
> a first switch node configured to connect to an external circuit;
>
> a second switch node configured to connect to the external circuit;
>
> a transistor device having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;
>
> a third switch node for receiving the control signal; and
>
> an impedance circuit connected to the third switch node and the third terminal of the transistor device, the impedance circuit configured with a sufficiently high impedance to reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch.

(emphasis added)

Applicants submit that the prior language of claim 1 did not, in fact, recite "result language," but rather recited a structural limitation of the circuit. Applicants respectfully assert that as implemented in claim 1, the use of the phrase "thereby" provides a positive limitation of the claim. Just as relative terms such as "substantially" do not *per se* render a claim indefinite, functional language, such as the use of the phrase "thereby" in claim 1, does not *per se* constitute non-limitations. This point is clear in view of *Pac-Tec, Inc. v. Amerace Corp.*, 903 F.2d 796, 14 USPQ2d 1871 (Fed. Cir. 1990), cert. denied, 502 U.S. 808 (1991), in which the Federal Circuit noted the impropriety of disregarding limitations that include

"adapted to," "whereby," and "thereby." *Pac-Tec*, 903 F.2d at 801, 14 USPQ2d at 1876; *See also*, *In re Venizia*, 530 F.2d 956, 189 USPQ 149 (CCPA 1976).

However, in the interest of furthering prosecution, Applicants have cosmetically amended claim 1 to highlight the functional characteristics of the transistor device in claim 1. Applicants respectfully submit that independent claim 1 is allowable over the '947 patent for at least the reason that the '947 patent does not disclose, teach, or suggest that the circuit connected to the third switch node and the third terminal of the transistor device is configured with "**a sufficiently high impedance to reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch**."

Applicants submit that the revised language of this claim does not recite "result" language. The claim, as written, recites the structure of a "transistor device" with the functional limitation of the transistor device being configured with "**a sufficiently high impedance to reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch.**" This point is clear in view of MPEP 2173.05(g), citing *In re Swinehart*, 439 F2d 210, 169 USPQ 226 (CCPA 1971), which states that there "is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper." Thus, the functional limitation in claim 1 is a positively-recited limitation that limits the scope of claim coverage.

The Office Action argues that "A1 has very high input impedance." This argument, however, ignores all of the cited claimed features by only focusing on the impedance of the circuit (A1, R1). Specifically, this argument ignores the fact that the '947 patent does not

disclose, teach, or suggest the impedance circuit connected to the third switch node and the third terminal of the transistor device having "**a sufficiently high impedance to reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch.**" In fact, the '947 does not disclose, teach, or suggest any relationship between the impedance of the circuit (A1, R1) and the parasitic capacitance between the first terminal and the second terminal of the transistor device. Rather, the '947 patent discloses using the circuit (A1, R1) within the control system 8, to amplify an input voltage (V_{CS}) to produce a control voltage (V_C) for the transistor device. As stated in the Abstract, "[t]his downscales the forward voltage characteristics of the circuit from those of the transistor." Thus, the circuit (A1, R1) disclosed in the '947 patent has nothing to do with the function of reducing the parasitic capacitance between the first terminal and the second terminal of the transistor device.

Accordingly, and for at least the reasons set forth above, independent claim 1 is believed to be allowable over the '947 patent. Furthermore, because claim 1 is believed to be allowable, dependent claim 2 (which depends on independent claim 1) should be allowable as a matter of law for at least the reason that claim 2 contains all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Applicants request that the Examiner reconsider and withdraw the rejection of claims 1 and 2 under 35 U.S.C. §102(b).

VI. Claims 3 – 5 are Patentable Over U.S. Patent No. 5,223,751 to *Simmons et al.*

The Office Action also rejects claims 3 – 5 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,223, 751 to *Simmons et al.* ("the '751 patent"). Specifically, the Office Action argues that Figure 3 of the '751 patent discloses the transistor circuits of

claims 3 – 5. The Office Action further alleges that the last three lines of claim 3 are merely "result" language and "thus may not be used to distinguish over the disclosure" of the '751 patent.

Applicants' claim 3 as amended, recites:

> 3. (twice amended) A transistor circuit for implementing a switch, comprising:
>
> a first switch node configured to connect to an external circuit;
>
> a second switch node configured to connect to the external circuit;
>
> a transistor device having a first terminal connected to the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal for controlling the electrical connectivity between the first terminal and the second terminal; and
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> an inverter circuit connected to the second terminal of the transistor device for reducing the noise at the first terminal of the transistor device, the inverter circuit configured to reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit by providing a voltage to the second terminal when the control signal engages the transistor device.

(emphasis added)

Applicants submit that the prior language of claim 3 did not, in fact, recite "result language," but rather recited a structural limitation of the circuit. Applicants respectfully assert that as implemented in claim 3, the use of the phrase "thereby" provides a positive limitation of the claim. Just as relative terms such as "substantially" do not *per se* render a claim indefinite, functional language, such as the use of the phrase "thereby" in claim 1, does not *per se* constitute non-limitations. This point is clear in view of *Pac-Tec, Inc. v. Amerace Corp.*, 903 F.2d 796, 14 USPQ2d 1871 (Fed. Cir. 1990), cert. denied, 502 U.S. 808 (1991), in which the Federal Circuit noted the impropriety of disregarding limitations that include "adapted to," "whereby," and "thereby." *Pac-Tec*, 903 F.2d at 801, 14 USPQ2d at 1876; *See also, In re Venizia*, 530 F.2d 956, 189 USPQ 149 (CCPA 1976).

However, in the interest of furthering prosecution, Applicants have cosmetically amended claim 3 to highlight the functional characteristics of the inverter circuit in claim 3. Applicants respectfully submit that independent claim 3 is allowable over the '751 patent for at least the reason that the '751 patent does not disclose, teach, or suggest that the inverter circuit connected to the second terminal of the transistor device is **"configured to reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit by providing a voltage to the second terminal when the control signal engages the transistor device."**

Applicants submit that the revised language of claim 3 does not recite "result" language. The claim, as written, recites the structure of an "inverter circuit" with the functional limitation of the inverter circuit being **"configured to reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit by providing a voltage to the second terminal when the control signal engages the transistor device."** This point is clear in view of MPEP 2173.05(g) citing *In re Swinehart*, 439 F2d 210, 169 USPQ 226 (CCPA 1971), which states there "is nothing inherently wrong with defining some part of an invention in functional terms. Functional language does not, in and of itself, render a claim improper." Thus, the functional limitation in claim 3 is a positively-recited limitation that limits the scope of claim coverage.

Applicants respectfully submit that independent claim 3 is allowable over the '751 patent for the additional reason that the '751 patent does not disclose, teach, or suggest that the inverter circuit connected to the second terminal of the transistor device is **"configured to reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit by providing a voltage to the second terminal when the control signal engages the transistor device."** The '751 patent makes no mention of configuring the inverter circuit, which is connected to the second terminal of the transistor device, to reduce

the parasitic effects of the transistor device. Claim 3 is directed towards a system designed to reduce noise injected to the external circuit at the first switch node. The claimed invention achieves this by configuring the inverter circuit to **reduce the parasitic effects of the transistors**. However, the voltage shifting device of '751 patent does not disclose, teach, or suggest any solution for reducing the parasitic effects of the transistor device by improving the function of the transistor-based switch.

Accordingly, and for at least these reasons, Applicants respectfully submit that independent claim 3 patently defines over the '751 patent and, therefore, is in condition for allowance. Furthermore, because independent claim 3 is believed to be allowable over the prior art of record, dependent claim 4 (which depends from independent claim 3) is allowable as a matter of law for at least the reason that claim 4 contains all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 3 and 4 in condition for allowance.

VII. Claims 6 – 8 are Patentable Over U.S. Patent No. 4,752,703 to *Lin*.

The Office Action rejects claims 6 – 8 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,752,703 to *Lin* ("the '703 patent"). Specifically, the Office Action argues that the '703 patent discloses the transistor circuits of claims 6 – 8.

Applicants' claim 6, as amended, recites:

> 6. (twice amended) A transistor circuit for implementing a differential switch, comprising:
>
> a first switch node configured to connect to an external circuit;
>
> a second switch node configured to connect to the external circuit;
>
> a first transistor device having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;
>
> a second transistor device having a first terminal connected to the second terminal of the first transistor device, a second terminal connected to the second switch node, and a third terminal configured to receive the control signal; and
>
> a third transistor device having a first terminal connected to the first terminal of the first transistor device, a second terminal connected to the second terminal of the second transistor device, and a third terminal configured to receive the control signal, the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit.

(emphasis added)

Applicants respectfully disagree with the assertion that the '703 patent discloses every feature of claim 6. Particularly, the '703 patent does not describe the transistor circuit as having a **"third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit"** as claimed. In contrast, the '703 patent is directed to reducing signal noise by connecting a dummy load to the switching circuit (col 3, line 45-47). The '703 patent does not describe using a third transistor's inherent parasitic capacitance and resistance to effectively reduce the overall characteristics of the transistor circuit. Rather, the '703 patent teaches the reduction of signal noise at nodes X and Y by introducing a dummy load at the X and Y nodes at the moment when the sourcing output current is switched to the sinking output current (col 3, 45-48). The reference discloses reducing the signal noise, not by a reduction in overall circuit capacitance,

but by effectively stabilizing the voltage at nodes X and Y by preventing node X from being pulled up to V_{DD} and preventing the voltage at node Y from being pulled down to V_{SS} (col 4, line 9-17). Therefore, Applicants respectfully submit that independent claim 6 is allowable over the '703 patent for at least the reason that the '703 patent does not disclose, teach, or suggest a transistor circuit as having a **"third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit."**

Furthermore, because independent claim 6 is believed to be allowable over the prior art of record, dependent claims 7, 9, and 10 (which depend from independent claim 6) are allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 6, 7, 9, and 10 in condition for allowance.

CONCLUSION

In light of the foregoing remarks and for at least the reasons set forth above, Applicants respectfully submit that all rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-4, 6-7, and 9-10 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.

Adam E. Crall
Registration No. 46,646

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
Suite 1750
100 Galleria Parkway N.W.
Atlanta, Georgia 30339
(770) 933-9500

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington D.C. 20231, on 11/27/02.

Stephanie Riley
Signature

ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

The following claims have been amended by deleting the bracketed ("[]") portions and adding the underlined ("___") portions.

1. (thrice amended) A transistor circuit for implementing a switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a transistor device having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a third switch node for receiving the control signal; and

[a] an impedance circuit connected to the third switch node and the third terminal of the transistor device, the impedance circuit [having] configured with a sufficiently high impedance to [prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch and thereby] reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device by preventing the third switch node from functioning as an alternating current (AC) ground during operation of the switch.

3. (twice amended) A transistor circuit for implementing a switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a transistor device having a first terminal connected to the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal for controlling the electrical connectivity between the first terminal and the second terminal; and

[a] an inverter circuit connected to the second terminal of the transistor device for reducing the noise at the first terminal of the transistor device, the inverter circuit configured to [provide a voltage to the second terminal when the control signal engages the transistor device to] reduce parasitic effects at the first terminal when the transistor circuit functions as an open circuit[, thereby reducing noise injected to the external circuit at the first switch node] by providing a voltage to the second terminal when the control signal engages the transistor device.

6. (twice amended) A transistor circuit for implementing a differential switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a first transistor device having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a second transistor device having a first terminal connected to the second terminal of the first transistor device, a second terminal connected to the second switch node, and a third terminal configured to receive the control signal; and

a third transistor device having a first terminal connected to the first terminal of the first transistor device, a second terminal connected to the second terminal of the second transistor device, and a third terminal configured to receive the control signal, the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit.